DESIGN AND VALIDATION OF LOW POWER AND HIGH EFFICIENCY CMOS LEVEL SHIFTER

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ABSTRACT

The most crucial design factors for system-on-a-chip design are power and performance efficiency. Numerous techniques were created to lower supply voltage and multiple supply voltages in order to reduce power and delay. Voltage level conversions across several voltage domains are required for different supply voltage configurations. The use to achieve this effect, voltage level shifter (LS) circuits are used. Low-core-voltage (LSV) circuits connect high-core voltage and low-core-voltage (HCV) systems, and vice versa. LS makes it easier for different parts to talk to one other. The problem is that most LSs have latency, according to the study. fluctuation as a result of high power dissipation and different current driving transistors. After a careful analysis of the literature, this research identifies the shortcomings and design features of contemporary LSs and projects their current status. The power consumption, processing speed, and various supply voltages in ICs are the main topics of this research. It is anticipated that the thorough literature research would open the door to resolving LS-related problems and difficulties and aid in the creation of effective low-power multi-voltage LSs for VLSI circuit design

Keywords: low power , Tanner 16nm, CMOS level shifter, High Performance

I.INTRODUCTION

Low power consumption is necessary for digital circuit design due to the quick growth of portable devices like smartphones and PCs. Reducing the supply voltage is One of the best methods for reducing the power usage of the system [1], [2], but it will also slow down the system. various functional modules run at various voltages thanks to the introduction of multi-voltage technology, which strikes a reasonable balance between performance and power consumption. As a result, the wide-range voltage conversion level shifter (LS) has to implement several function domains at various source voltages. Two crucial aspects of an LS are its power consumption and propagation latency. Low-power systems need quick and energy-efficient LSs because to the growing complexity of the System-on-Chip. Fig. 1 depicts three common LS kinds. DCVSLS is a level shifter based on a differential cascade voltage switch. The networks for pull-up and pull-down are in competition with one another. and the argument is stronger since the voltage conversion fails because The input voltage falls below the threshold.. Fig. 1 shows another traditional LS that

uses CMLS stands for present mirror structure. The pull-up network's strength is thus constrained. This structure's primary benefit The pull-up and pull-down have very little competition over the DCVSLS. networks; however, it also has the drawback of having an inability to fully shut MN1 and MP1, which results in a high static current. Several LS circuits have been described to address these issues in the two traditional LS architectures [3]. However, there are further issues with the present limiter's insertion, such as output swing reduction, which will raise the following stage buffer's static power. Although a smaller swing buffer is used in this LS structure [4] in Fig. 2 to reduce battery use, The difference in voltage between MP3 files is inadequate for regulating the static current. Figure 2 illustrates the output as indicated by LS [5]. However, The MP2 transistor's sluggish closing speed leads to a significant power consumption overhead in MP4 and MN2's current course during high-to-low transitions. Power input requirements are increased because to the accelerated transition conflicting currents at N2 cause input levels to range from high to low. By including auxiliary bias circuits, the LS structure [6] resolves the problem of decreased swing. The low-voltage cascode assembly is shown in Figure 2 to demonstrate its integration [7]. When operating at low voltage, Node NP will still see contention current creation, even though the transition will be slower and power consumption will increase, especially in the sub-threshold region. The design [8] includes an error-correcting circuit, as shown in Fig. 2, to make spotting the low to high transition simpler. It takes a long time for the input to get from high to low because of the complicated pull-up method. Leakage current via MN1, MP1, and MP4 also contributes to higher power usage. The best design for separating pull-up and pull-down channels is a current control circuit that is triggered by logic mismatch [9]. Nevertheless, it is expected that the contention current from MNL7 and MNL8 to the VSS would increase power consumption and prolong the transition time when the input goes from high to low. A number of designs are shown. The proposed LS uses a voltage hysteresis transistor to reduce the internal node voltage volatility. Additionally, mixed threshold transistors enhance propagation latency and voltage conversion range by making the pull-up and pull-down networks more competitive. While charging node N2, a defective shut-off transistor disables the pull-down network, reducing the leakage current in the LS circuit.. These innovative methods allow for the suggested LS may perform quick voltage conversion and ultra-low power. This brief's remaining sections are structured as follows: Section II provides an example of the suggested LS. Section III displays the outcomes of the simulation. Section IV displays the comparisons and measurement findings. Section V concludes this brief. Section I provides an overview of this research. Section II: Literature Review. Section III: Present Method 1. While the fifth part offers the conclusion

and future goals, the fourth section sets out the suggested technique.

II.LITERATURE SURVEY

The business and scientific community are becoming more interested in ultra-low power VLSI circuits. In fact, a lot of current and future applications specifically depend on the availability of energy-autonomous, very compact sensor nodes. Ambient intelligence, wearable technology, smart grids, wireless sensor networks, biomedical and implanted devices/networks, pollution and plant monitoring, and smart warehouses

are a few examples of these applications [1]–[5]. Lifetime and size are the primary motivators in the context of these applications and the associated technologies [6]–[8]. Although it is now hardly achievable, a battery lifespan of many years or decades would be ideal. Future nodes aim to be millimeters or smaller [1], [2], and several prototypes are now on the market [9]. The energy storage/scavenging device (which usually determines the size of the whole node) and the node consumption impose strict limitations on both lifespan and size. Since CMOS technology has advanced much more quickly than battery technology, a lot of research has gone into rapidly lowering node consumption, which may now be far lower than the microwatt for the aforementioned applications. According to Bell's rule, computers have historically shrunk by 10 to 100 pieces every ten years [6], [7], although innovation will be necessary to maintain energy-autonomous operation. In order to conserve energy, noncritical blocks continue to run at lower supply voltages (VDDL) even in the sub-threshold zone, whilst time-critical blocks run at higher voltages (VDDH) to match the performance parameters. A large number of VDD systems need trustworthy level shifter circuits to provide correct interfacing across different voltage domains without compromising the design's overall robustness. Two topologies characterize state-of-the-art level shifters: current mirror (CM) and cross coupled (CC). Nevertheless, their static power consumption is often somewhat large. The aforementioned problems with CC and CM-based topologies have been the subject of several recent proposals for solutions. For up-conversions from very low-voltage domains, PUNs reduce current contention in CC-based systems, which improves switching speed and energy efficiency. Furthermore, a split-input inverting buffer's output step improves power efficiency. In order to circumvent voltage loss and inadequate feedback restrictions, conventional CM-based level shifters might benefit from using mixed-threshold voltage (VTH) devices, as proposed in [8]. An enhanced switching speed is achieved with the use of pass transistor-based circuitry in [9], and a reduced-swing output buffer design is able to save standby power. To enhance energy, latency, and static power utilization, an alternate solution is presented in [10]. This strategy involves a self-

controlled current limiter that can transition voltages between deep sub-threshold and above-threshold domains. As can be seen in [11] and [12], CM-based topologies also make advantage of the split-input inverting buffer to reduce the output stage static current. This video demonstrates a low-voltage level shifter that makes use of a self-biased low-voltage cascode CM technique. and an inverted output buffer with split-input. The authors believe this to be the first study to use silicon measurements to suggest and validate such a CM architecture for level shifter design

III.EXISTING METHOD

A novel voltage conversion circuit combining an output buffer and a current mirror is proposed for use in the LS, as shown in Figure 1. The recommended LS transistor size is shown in Table I. By constructing a fast pull-down network using With a low-threshold transistor MN5, this circuit allows for a [8]quick reduction in the transmission delay and the pull-down of N2.It is also important to consider the pull-up network's quick shutdown for energy saving

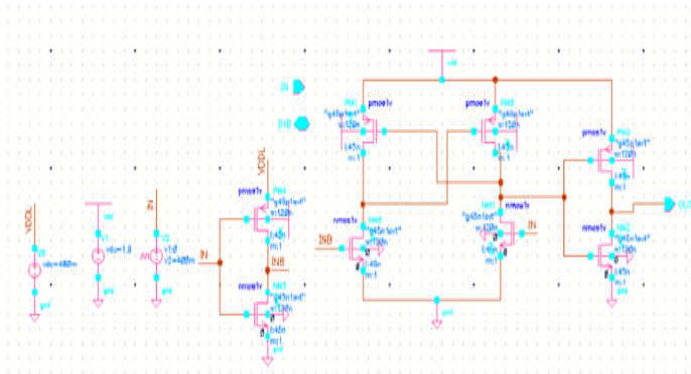

Fig .1 Existing level shifter with DCVS-Based LS

In order to quickly close the current mirror, the transistor MN3 is positioned after N2, the internal node, has a full charge. Fig. 4 shows this as VDSL becomes high and VSS becomes low. Additionally, the pull-down network is enhanced by the use of low-threshold transistors in the construction of both the MN1 and the MN2, as well as the internal node is charged by the current mirror N2 via the MP2. But still

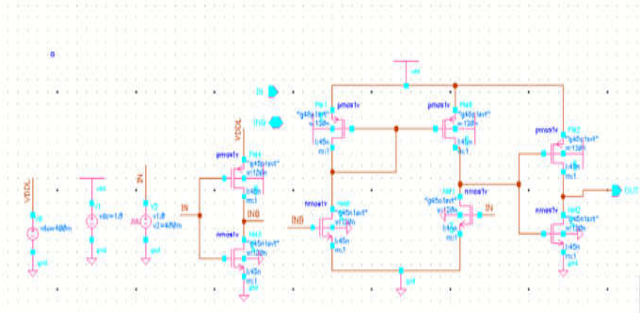

Fig .2 schematic of Current mirror based LS

Typically, the input voltages of traditional current mirror LS[9] networks either reach or drop below the level where the pull-down networks MN1 and MN2 cannot discharge. N1. With this change, the N2 will charge for less time, which reduces the swing problem and boosts the buffer's static current for the next step

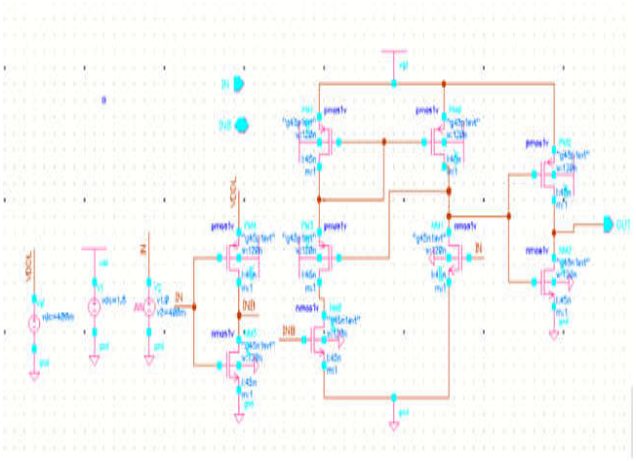

Fig.3 current mirror schematic based on wilsion approach

Adding a voltage hysteresis transistor, MP3, solves the issue by decreasing MP1's strength, oftransistors near to VDDas seen in Fig. 4. illustratesMP2 may charge the node N2 more quickly because of the current coming from MP2 and the N1's capacity to hold a lower voltage. In the meanwhile, MN5's supply is linked to VDDL [10] in a similar way, shutting MN5 off entirely and stopping current from leaking. This design could completely stop the leak. Regarding Energy difference at N2, Fig. 4 compares the suggested LS with the others. Using MP3 greatly lessens the swing issue. Additionally, there includes a leaking tuned to cut off transistor (MN3) to save energy. At low N3 and high N2, Both the current mirror and the MN3 are currently closed. Details of how the proposed LS interacts with inputs that oscillate between high and low, using the VSS (low) input rather than the VDDL (high) input. Displaying several waveforms at internal node N2, including the intended LS. The output waveform of the proposed LS is one such example. Leakage current occurs in the circuit when the input voltage is low. 1.2 V at 0 V input is VDDH, [11]which is the distribution of power consumption with and without MP7. Figure 5 displays the resultant waveform. In Figure 4, it is shown It is possible to disable the current mirror's leakage current at low input voltage (VSS) by modifying the voltage at node N4. Eventually, the leakage current will decrease when the voltage reaches VDDL. With the addition of a voltage hysteresis transistor MP7, raising the voltage of node N4, which is located between MN1 and MN2, results in a decrease in leakage current and a robust closure of the stacked NMOS. Because of this, the mirror is now entirely closed. Compared to the stacked NMOS MN1 and MN2, there is still a noticeable power gain, even if the MP7 would cause an increase in power usage.[12] The outcomes of the simulation are shown.in Figure 5. When compared to the leakage power of the traditional stacked NMOS without MP7, the leakage power from VDDH is much lower and the overall power consumption includes MP7.

IV.PROPOSED METHOD

Large power consumption per unit space has increased as [13]a result of digital integrated circuits' (ICs') increasing size and functional density. Aside from speed and space, one of the main design restrictions is the IC's power consumption. The three types of power consumption in VLSI are leaky, dynamic, and static. The dynamic power

consumption is based on the frequency of operation and results from the load capacitance altering at various voltages. The straight The static electricity originates from a short circuit connection between the VDD and ground. Because leakage current comes from substrate-injection and sub-threshold regimes, reducing leakage power may get sufficient attention.. Power supply voltage scaling may lower system-level power consumption, but it also introduces issues like as voltage swing, leakage currents, and inadequate noise margins. Additionally, circuit architecture affects speed and latency. For VLSI designers,[14] power consumption has become the most important design restriction in the context of portable and handheld devices, along with battery charge frequency. Along with the expense of packaging, power consumption and reliability issues also grow.

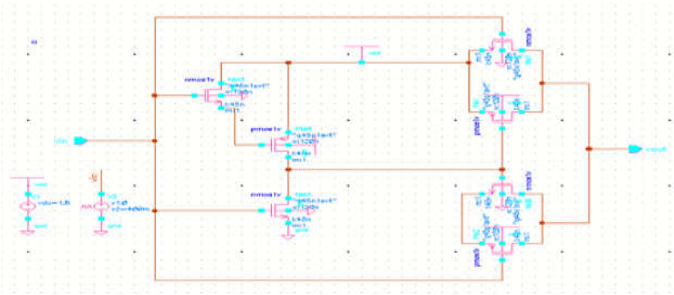

Fig.4. schematic of proposed method

In transmission gate LS designs, the transmission gate serves as the [15] fundamental circuit component. Since its ON resistance is smaller than the NMOS's, the output has a reduced transition The LS is operational far below the sub-threshold regimes. For the LSs, 160 mV is the absolute minimum input level that will work. Figure 4 shows that the Transmission Gate Level Shifting buffer has an output node voltage (VOUT) of 1V. Given that the LS's output voltage grows, its slew-rate stays the same. The time, which minimizes latency and eliminates the need for contention mitigation. Transmission gate LS lowers leakage and dynamic power usage output node gets less current because of the TG Level shifting buffer. Improved dynamic energy efficiency and performance are the results of a higher buffer output value and a [16] faster output slew rate, made possible by the lack of contention and the short circuit current flow requirements.

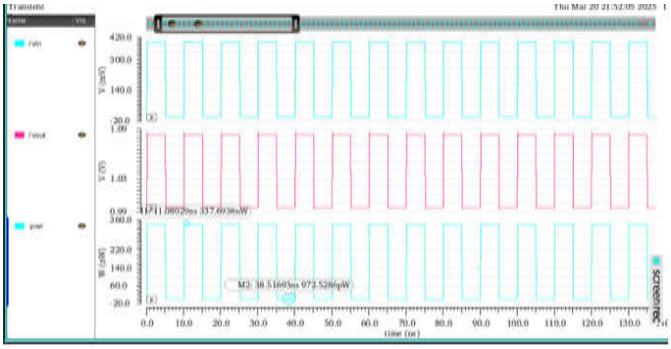

FIG.5. Power analysis of proposed method

This graphic illustrates the power analysis of static and dynamic power. Static power consumption by the proposed method is 337.69 Nano watt. Dynamic power consumption by the proposed method is 972.52 Pico watts. And average power consumptions isaround 166.9 Nano watts.

V.CONCLUSION AND FUTURE SCOPE

Using very low input voltages as a starting point, this brief examined modern voltage level-shifting buffer architectures that may increase threshold voltages. This voltage level shifting circuit for transmission gates is more efficient than the others because the pull-down device drastically reduces the voltage at the output node and the pull-up device drastically reduces the current flowing through it.. However, the pull-down circuit's strength also significantly increases. Results from simulations provide good support for power and performance measurements. When compared to previous works, the transmission gate voltage level changing circuit is particularly noteworthy for its power usage

REFERENCES

[1] M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 59, no. 1, pp. 3–29, Jan. 2012, doi: 10.1109/TCSI.2011.2177004.

[2] J. Lee et al., "A self-tuning IoT processor using leakage-ratio measurement for energy-optimal operation," IEEE J. Solid-State Circuits, vol. 55, no. 1, pp. 87–97, Jan. 2020, doi: 10.1109/JSSC.2019.2939890.

[3] S. Lütkemeier and U. Rückert, "A subthreshold to above-threshold level shifter comprising a Wilson current mirror," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 9, pp. 721–724, Sep. 2010.

[4] V. L. Le and T. T. Kim, "An area and energy efficient ultra-low voltage level shifter with pass transistor and reduced-swing output buffer in 65-nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 5, pp. 607–611, May 2018.

[5] S. Kabirpour and M. Jalali, "A power-delay and area efficient voltage level shifter based on a reflected-output Wilson current mirror level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 2, pp. 250–254, Feb. 2020, doi: 10.1109/TCSII.2019.2914036.

[6] H. You, J. Yuan, W. Tang, S. Qiao, and Y. Hei, "An energy-efficient level shifter for ultra low-voltage digital LSIs," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 3357–3361, Dec. 2020, doi: 10.1109/TCSII.2020.2980681.

[7] L. Fassio et al., "A robust, high-speed and energy-efficient ultralowvoltage level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 4, pp. 1393–1397, Apr. 2021, doi: 10.1109/TCSII.2020.3033253.

[8] K. Kim, J. Y. Kim, B. M. Moon, and S.-O. Jung, "A 6.9-μm2 23.26-ns 31.25-fJ robust level shifter with wide voltage and frequency ranges," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 68, no. 4, pp. 1433–1437, Apr. 2021.

[9] M. N. Sharafi, H. Rashidian, and N. Shiri, "A 38.5-fJ 14.4-ns robust and efficient subthreshold-to-suprathreshold voltage-level shifter comprising logic mismatch-activated current control circuit," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 70, no. 6, pp. 1906–1910, Jun. 2023, doi: 10.1109/TCSII.2023.3237083.

[10] H. Jeong, T.-H. Kim, C. N. Park, H. Kim, T. Song, and S.-O. Jung, "A wide-range static current-free current mirror-based LS with logic error detection for near-threshold operation," IEEE J. Solid-State Circuits, vol. 56, no. 2, pp. 554–565, Feb. 2021, doi: 10.1109/JSSC.2020.3014954.

[11] E. Låte, T. Ytterdal, and S. Aunet, "An energy efficient level shifter capable of logic conversion from sub-15 mV to 1.2 V," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 11, pp. 2687–2691, Nov. 2020.

[12] Z. Yong, X. Xiang, C. Chen, and J. Meng, "An energy-efficient and wide-range voltage level shifter with dual current mirror," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 25, no. 12, pp. 3534–3538, Dec. 2017.

[13] S.-C. Luo, C.-J. Huang, and Y.-H. Chu, "A wide-range level shifter using a modified Wilson current mirror hybrid buffer," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 61, no. 6, pp. 1656–1665, Jun. 2014.

[14] R. Lotfi, M. Saberi, S. R. Hosseini, A. R. Ahmadi-Mehr, and R. B. Staszewski, "Energy-efficient wide-range voltage level shifters reaching 4.2 fJ/transition," IEEE Solid-State Circuits Lett., vol. 1, no. 2, pp. 34–37, Feb. 2018, doi: 10.1109/LSSC.2018.2810606.

[15] E. Maghsoudloo, M. Rezaei, M. Sawan, and B. Gosselin, "A highspeed and ultra-low-power subthreshold signal level shifter," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 64, no. 5, pp. 1164–1172, May 2017.

[16] M. Lanuzza, F. Crupi, S. Rao, R. De Rose, S. Strangio, and G. Iannaccone, "An ultralow-voltage energy-efficient level shifter," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 64, no. 1, pp. 61–65, Jan. 2017.