# DESIGN AND VALIDATION OF LOW POWER AND HIGH PERFORMANCE 4X4 ARRAY FOR ADDRESS GENERATION APPLICATIONS

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**ABSTRACT**

This project uses a 2x4 row decoder with 10T SRAM cells to construct a 4x4 memory array. Implementing a small, effective memory system that works well for high-speed, low-power applications is the goal. In order to pick one of the four word lines and get access to certain rows in the memory array, the design includes a 2x4 decoder. The 10T SRAM architecture, which is used to create each memory cell, has benefits over traditional 6T SRAM cells in terms of smaller size and easier arrangement. 16 memory cells organized in 4 rows and 4 columns make up the 4x4 memory array. In order to read from or write to the chosen row, the decoder needs a 2-bit address input. It then activates the matching row line. The addition of sense amplifier logic and column selection completes the read/write operations. Using the proper VLSI design tools, the whole design is simulated and its speed, area, and power consumption are examined. This study illustrates the trade-offs between cell density, power, and performance and shows that 10T SRAM cells are feasible to use in small-scale memory arrays. CMOS 45nm Cadence technology has been used to verify the proposed design. Applications needing small, low-power memory solutions and embedded devices are a good fit for this architecture.

*Keywords: low power, high efficient, CMOS Transistors, 4x4 Memory array*

## I.INTRODUCTION

People's lives have been simpler and better because to the numerous helpful technologies this business has provided, like satellite phones, military surveillance, navigation systems, tracking systems, and more. For tasks including engine management, control and guiding, and inertial navigation, planes often employ microprocessors. These computers are getting a lot of cores to improve their performance. When there are more cores, more RAM must be cached [2]. Consequently, SRAM cells—cache memory—are vital for maximizing the power, capacity, and speed of the CPU. Space-borne, high-energy particles change how our brains' memory circuits work [3]. A semiconductor memory board or other integrated circuit may produce two new electron and hole pairs when a powerful particle hits its base. In the direction from the substrate/n-well to the diffusion zone, there is a bias that is backwards.

is what this is known as [4, 5]. Additionally, since technology is developing so rapidly, there is less space between components on an integrated circuit [6]. This might result in a single-event upset as a single ion hit could have an influence on several nodes. They have used triple modular redundancy (TMR) to address the memory impact of SEUs. In this system, the majority determines which of the three memory cell copies shows the right number [7, 8]. Two copies will vote for you if you flip one, and the outcome will be the same. However, most designs shouldn't employ this method since it consumes a lot of power and space [8, 9]. Error correction codes (ECCs) are another method to mitigate the impact of SEUs. However, since ECCs need additional devices and backup circuits for encoding and decoding, they require a lot more time, space, and power. Because they use less time, space, and power than ECCs, soft-error-aware SRAMs are superior. Additionally, it's preferable if the SRAM cell can recover from disturbances as well as SEUs. The primary cause of nanoscale memory' decreased reliability is rays. Single event upsets (SEUs) may result from them. This paper presents a novel approach with a good layout-topology that is based on the SEU physics process. Complementary Metal Oxide Semiconductor (CMOS) technology at 65 nm suggests a secure memory cell. In addition, we compare the reading and writing times, power consumption,

## II.LITRATURE SURVEY

These are significant problems because they reduce nanoscale memory systems' accessibility and dependability. [1] through [3]. Simplified Complementary Metal Oxide Semiconductor manufacturing has reduced source voltage and node capacitance, making memory cells more vulnerable to radiation particles. (CMOS) technology [4–7]. An SEU has the ability to abruptly stop electronics from functioning and alter the data stored in memory cells [4]. Because they might be resolved at the subsequent write or restart, SEUs are often referred to as ".s" [4, 5]. In some crucial memory conditions, heart defibrillators and other medical equipment may be both beneficial and detrimental. The next step is to take the appropriate precautions to shield memories from SEUs in the presence of radiation. Triple modular redundancy (TMR), which reduces the harm that SEUs do to storage, has been the solution. TMR selects the correct number and distributes it using a majority vote and three copies of memory cells [9]. One copy turned over will still result in the correct outcome as long as the other two copies vote. However, the approach demonstrates that TMR would need to pay excessively for power and space, making it unusable for the majority of designs [9, 10]. Another method of strengthening a circuit to prevent SEUs is to utilize radiation-hardened

memory cells. [11] Demonstrated that a novel NMOS stacked (NS) memory cell could use a stacked structure to return from 0 to 1 SEU. Section I provides an overview of this research. Section II: Literature Review. Section III: Present Method 1. While the fifth part offers the conclusion and future goals, the fourth section sets out the suggested technique.

III.EXISITING METHOD

The plan and the like The layout and construction of 12T are shown in Figure 1. Twelve nodes: S1 and S0 on the inside, WL and WWL on the outside, and Q and QB on the inside, make up the network. Through the regulation of access transistors N7 and N8, WL establishes a connection between storage nodes Q and QB and BL and BLB. Turning on the access transistors (N9 and N10) allows WWL to connect the internal S1 and S0 nodes to respective BL and BLB bit lines. View SARP12T and all comparison cells with Q = 1 and QB = 0 in turn. So, S1 and S0 are true for 1 and 0, respectively. What follows is an explanation of how the SARP12T works and an examination of the SEU recovery. Core Responsibilities These are the SARP12T procedures that are planned. By grounding WL and WWL, the Hold Mode disables both sets of access transistors. To decrease read latency when in hold mode, pre-charge the bit lines with VDD. While the cell is in the hold state, only P1, N2, N3, and N6 will be ON, while all the other transistors in the scenario will be OFF. This is how By bringing BL to GND, nodes Q and S1 are also brought down by N7 and N9, respectively. As S1 deactivates nodes 2 and 3, node Q activates node P2 and deactivates node N6. Meanwhile, nodes QB and S0 are being pulled up by BLB via nodes N8 and N10, respectively. This causes node QB to activate N5 and deactivate P1. N1 and N4 are also activated and deactivated by node S0.

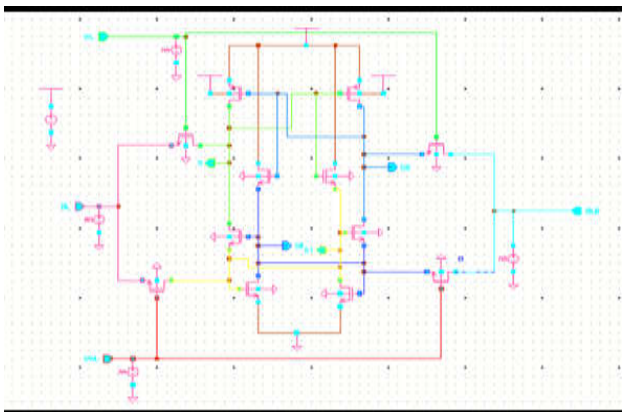

Fig.1. SRAM design using 12 Transistor

The potential difference between Q and QB is amplified because to the cross-coupling between P1 and P2. N3 and N4's cross-coupling amplifies the difference in potential between S0 and S1. The process of writing has been completed successfully. Although the read operation connects WL to VDD, it disables WWL. Consequently, N7 and N8 are set to active, while N9 and N10 are left to off. Just type in "0." VDD is read using bit-lines that have been pre-charged. N8, N2, and N3 have all been affected by BLB's discharge. Conversely, with N1 and N4 off, BL remains at VDD. The stored data may be

detected by a sensing amplifier that completes the readout as soon as the voltage difference between BL and BLB reaches 50 mV..

2) Writing: During this writing process, the WL and WWL word lines are both in use. Access transistors N7/N8 and N9/N10 are activated (turned on) as a consequence. To alter the data in memory (i.e., to put zero in Q), BLB is brought up to VDD while BL is taken low, to GND. Because BL is grounded, it pulls down node S1 by N7 and node Q via N9. While node Q activates node P2 and deactivates node N6, node S1 disables nodes N2 and N3. Currently, BLB is fetching nodes S0 over N8 and QB over N10 at the same time. Consequently, Node QB will turn N5 on and P1 off. Similarly, N1 and N4 are turned on by node S0. The possible disparity between Q and QB increases when P1 and P2 cross-couple. S1 and S0 have a stronger potential difference due to cross-coupling between N3 and N4. The write procedure is therefore completed successfully. As WWL is connected to VDD during the read process, it is disabled. So, N7 and N8 are ON, while the other two transistors (N9 and N10) are OFF. Bit-lines are already attached to VDD for reading purposes. Therefore, N8, N2, and N3 are the substances that drain BLB. Conversely, with N1 and N4 disabled, BL remains at VDD. A sensing amplifier (not shown) can read the data saved when the voltage difference between BL and BLB is 50 mV

## III.PROPOSEDMET

## HOD

Figure 2 displays the proposed SE10T SRAM cell's schematic along with the different control signals' current states. As previously mentioned, the storage nodes Q and QB are responsible for preserving the data, while M1 through M7 make [10] up the cross-coupled connectivity of inverters. M8: read word line (RWL) gates the read access transistor, M8. M8: write word line (WWL)

gates the write access transistor, M9. Read bit line (RBL)/write bit line (WBL) controls the reading and writing of data to and from the cell job. Q B is in charge of M 10, a read-assist transistor. When writing and holding zero, this transistor also contributes to the complete discharge of the storing node Q.

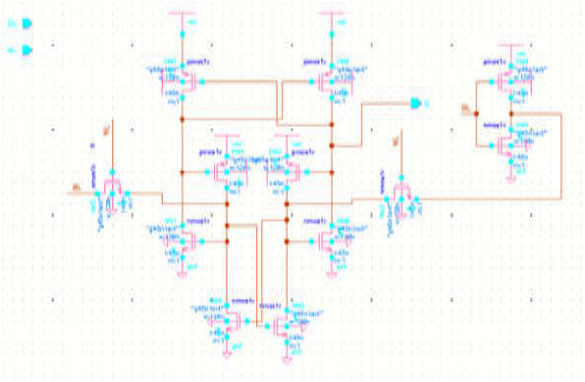

Fig.2. SRAM design using 10 Transistor

Four locked storage nodes are interconnected in the schematic model. This configuration aids in the prevention of faults [9]. Both the PMOS and NMOS transistors' gates include a storage node in a

conventional 6T SRAM. Consequently, cell data flipping results from any event transition (SET) that weakens the pull-up of PMOS or pull-down of

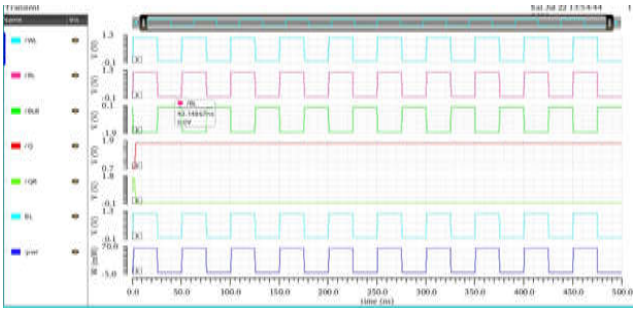

Fig.3. Proposed design of 10T SRAM using cadence virtuoso environment

NMOS by intensifying the associated pull-down of NMOS or pull-up of PMOS, respectively.

**A.POWERANALYSIS**

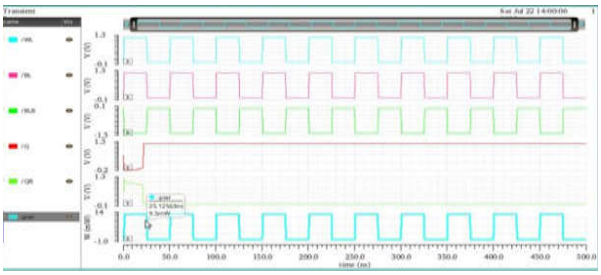

Fig4.Dynamicpower analysis

The 10T SRAM interlocked structure, however, has a storage node at the gate of two NMOS transistors or a pair of [12] PMOS transistors. In this method, a

**IVSIMULATIONRESULTS**

**A )Designof4x4memorywith 2x4decoder**

SET may either weaken the NMOS transistors' pull-down or the PMOS transistors' pull-up. However, it has no direct effect on the soft-error indemnity of other transistors of the same strength. Assume that a radiation particle collides with node B in Figure 2, momentarily lowering the potential there. This SET has the ability to reduce N1 and N4[13] pull-down. However, because P1 and P4 are unaffected by this noise, the voltages of A and D only slightly shift. The supply level results from this, since the voltage eventually recovers at point "B." The original cell data will be unaffected by this SET.

Table: 1.Comparisonbetween12Twith 10T

| S.NO | Technology | Methodology | No: Transistors | Dynamic Power | Static Power | Avg Power | Delay |
|---|---|---|---|---|---|---|---|
| 1 | 90nm | SARP12T | 12 | 4.463 | 8.20mw | 9.60mw | 100.01n |
| 2 | 45GPDK | 10TSRAM | 10 | 9.56mw | 29.07pW | 6.40mw | 55.7219p |

To move data in and out of the device, a memory unit consists of a collection of storage cells and associated circuits. Random access memory (RAM) is made up of memory cells that may be used to send or receive data to any random location. Memory unit block diagram Internal organization: An underlying structure of MXN binary [14] storage cells and the circuitry to decode down to the access of individual words make up a random-access memory with m words of n bits apiece. The Three is the input, while one binary cell is the output. Before the reda/write [15] input determines the mode of operation the cell is in when chosen, the choose input chooses which cell to read or write to. With a read/write input of 1, the flip-flop provides a route to the output terminal for the read operation. By establishing a communication link between the input terminal and the flip-flop, a 0 in the read/write input allows for write operations. The layout of a 4x4 memory with a 2x4 decoder [16]With the use of a 2x4 decoder, a 4x4 memory architecture employs the decoder to choose one of the four memory locations, after which the data is either read or written to the memory location.

B) Required Components

1. 2x4 Decoder: The 2-bit input will choose which of the four lines to turn on.

2. 4 Locations: There will be 4 bits in each memory location. Each memory location may have a 4-bit wide register.

binary cell is one of the basic building parts of a memory unit.

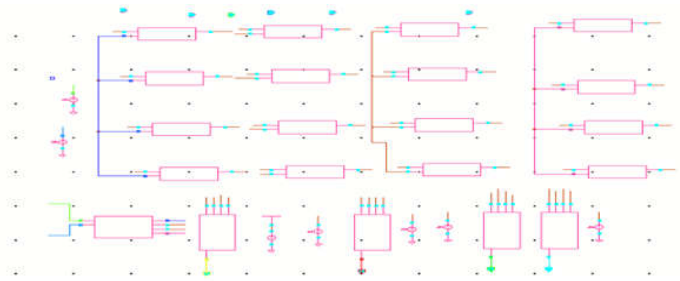

Fig 5. Simulationof4X4Memoryschematic

3. Write Enable Logic: A control signal that permits writing information to the designated memory address.

4. Data Bus: To read or write data to the RAM, use a 4-bit wide data bus.

The logical construction of a tiny 4X3 RAM is as follows. It consists of 12 binary cells with 4 words, each consisting of 3 bits. The binary cell with its three inputs and one output is located in each now-labeled BC block. The block diagram of a binary cell. It would need two address lines to have a four-word memory. A 2*4 decoder receives two inputs and allows the user to choose one of the four words. To enable the decoder, use the memory decoder input. When memory enable is set to zero, no memory words are selected and all decoder outputs are zero. Upon setting the memory enable to 1, the selection of one of the four words will be contingent upon the contents of the two address lines. It is

necessary to choose a word before the read/write input determines the action.

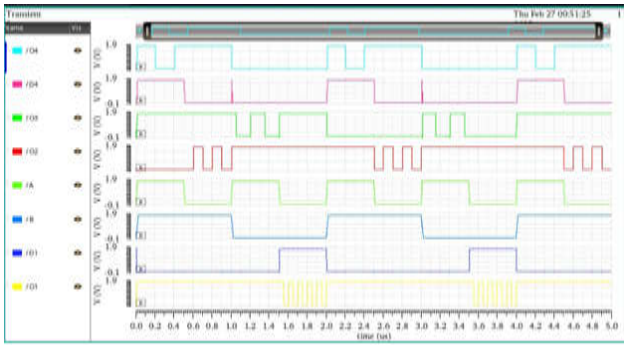

Fig. 6.simulation result of 4X4 Memory using 2X4 Decoder.

to Larger Memories: By using optimized cell arrays and higher-order decoders, this architecture may be expanded to handle larger memories (such as 8x8, 16x16). Power Optimization: Additional methods to cut down on power use include dynamic voltage scaling, clock gating, and power gating

## IV.CONCLUSION & FUTURESCOPE

This project successfully used a 2x4 decoder for address selection in the construction of a 4x4 CMOS memory unit. In order to enable one of the four memory rows depending on the 2-bit input address, the decoder is essential. Because CMOS logic ensures low power consumption and strong noise immunity, the architecture is effective for small-scale integrated memory systems. Schematic simulations were used to verify the design, ensuring that all memory cells could be read and written correctly. The use of a 2x4 decoder facilitated a structured and modular approach to memory architecture by streamlining address management and lowering circuit complexity. Scali

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