HIGH SPEED AND HIGH FREQUENCY GENERATION OF CMOS BASED VOLTAGE RING OSCILLATOR DESIGNED AT K BAND RANGE APPLICATION.

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ABSTRACT

There are many different designs for oscillators, and both active and passive parts have advantages and disadvantages. However, advancements in mobile communication technology have made interoperability and low power consumption more crucial. These oscillators waste minimal power, are compact, and have a wide tuning range. This study presents a novel kind of ring oscillator known as a voltage-controlled oscillator (VCO) composed of complementary metal oxide semiconductors (CMOS). The proposed design combines aspects of a current-starved ring oscillator with a negative-skewed delay technique to achieve maximum efficiency. With a supply and control voltage of around 5 V, the device can function at frequencies in the K-band range. The proposed method uses 5.0 mW on average, 5.62 mW dynamic, and 5.0 mW static power. The proposed method may generate a frequency of 21.66 GHz in the K Band area. We validated the design using the Cadence Virtuoso environment 45 GPDK. By carefully selecting the passive components, the proposed design offers a workable solution to the issues of high-frequency, low-power applications, meeting the needs of modern communication systems.

keywords — Very Large-Scale Integration (VLSI), CMOS RING oscillator with seven stages and a frequency range K-band.

I.INTRODUCTION

RF circuits are defined as working at higher frequencies than analogue circuits, which often employ radio signal transmission frequencies. Using frequency domain analytical techniques, such as Fast Fourier transforms, is necessary for RF circuit analysis. Because of this, RF designers may use carrier and harmonic frequencies to build circuit models. Additionally, frequency domain study may reveal frequency-dependent issues such as noise, interference, and waveform accuracy. Engineers conduct a great deal of study when they encounter problems while designing for radio frequency. Oscillators are an essential component of all communication systems [1]. The basis for producing a clock signal is an oscillator. Any electrical circuit's control and tracking depend on a clock signal. Regardless of the kind of oscillator, the relationship between a control voltage and the generated frequency controls how a VCO operates. 'ϋo' indicates the zero voltage (Vc=0) frequency, while 'kvco' indicates the VCO's sensitivity or gain. Section I provides an overview of this research. Section II: Literature Review. Section III: Present

Method 1. While the fifth part offers the conclusion and future goals, the fourth section sets out the suggested technique.

II. LITERATURE SURVEY

Make sure you have the appropriate template for the size of your paper first. The fundamental component of an oscillator is a positive feedback network, as shown in Figure 1. A positive feedback loop is a fundamental component of many engineering systems. This system would oscillate only under Barkhausen conditions. Previous methods give the closed-loop benefit. Ring oscillators and tank circuit oscillators are the two varieties of voltage regulated oscillators (VCOs). The tank circuit and a few other parts are what constitute a VCO. All VCOs [3] function in accordance with the Supplay Voltage, which determines the relationship between a control voltage and the output frequency. While 'kvco' represents the VCO's sensitivity or gain, 'ϋo' specifies the frequency at which the voltage is zero (Vc=0). Since the applied voltage and frequency in a voltage-controlled oscillator are directly proportional, changing the voltage will have the same impact as changing the frequency. There are two kinds of voltage control oscillators: a tank circuit-based oscillator and a ring oscillator [4]. The operation of the tank oscillator requires several modifications in order to act as a VCO.

III. EXISTING METHOD

Accuracy and Precision in Oscillation: Process variations, temperature swings, and supply voltage fluctuations make it challenging to get a stable and precise oscillation frequency with CMOS [5] ring oscillators.

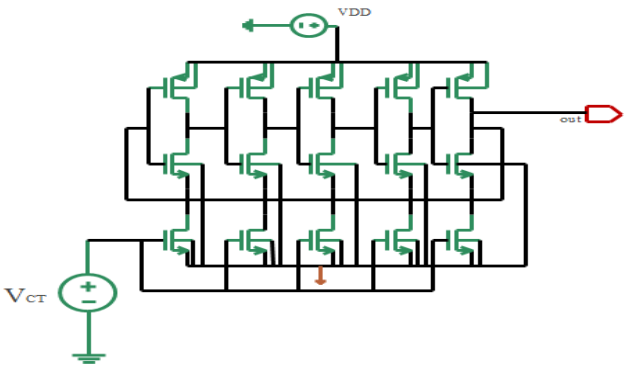

Fig.1.Schematic of current starved CMOS ring oscillator

Figure [2] describes the operation of negative skewed CMOS ring oscillator. Due to the need for extra stages or scaling to achieve high-frequency oscillation, the chip area might become constrained. A negatively skewed ring oscillator is a variant of a regular ring oscillator that purposefully introduces negative skew, which is the presence of delay components that cause signals to arrive sooner than anticipated in some routes. Although this isn't a phrase you'd see in a textbook, it's invaluable in the design of bespoke digital or analog ICs for tasks like controlling phase relationships or making sure there are smaller timing gaps. By adjusting the gate of the current-limiting transistors with a bias current or control voltage, the oscillation frequency and delay of each inverter stage may be fine-tuned. In order to facilitate comparison, the following are the disadvantages of negatively skewed ring oscillators and current-starved ring oscillators. Critical in communication systems, a low frequency range, inverter starvation increases delay variability, jitter, and phase noise. Accurate biassing circuitry is

necessary to regulate the current mirrors or bias transistors, since the delay is dependent on current sources and any change in VDD or threshold voltages might result in substantial frequency drift. Due to their temperature sensitivity, current mirrors might compromise oscillator stability if not corrected. Reducing the voltage swing by current restriction may result in slower transitions and smaller noise margins. The suggested approach is the greatest option for expanding the operating frequency range at high frequencies as it eliminates the aforementioned issues.

A CMOS ring oscillator operating in the K band is seen in the schematic below, which is based on the suggested design [6]. The performance of the proposed schematic has increased by the chain of inverters with optimization of transistor length. Reliability has been achieved by voltage process variations. To enhance the accuracy the proposed method has been adopted by 7 stages that's is hard number stages. To increase precession the proposed method developed with good biasing techniques. To minimize the power consumption the optimization of transistor length play a important role. To reduce the delay in ring oscillator , reduce the number inverter stages.

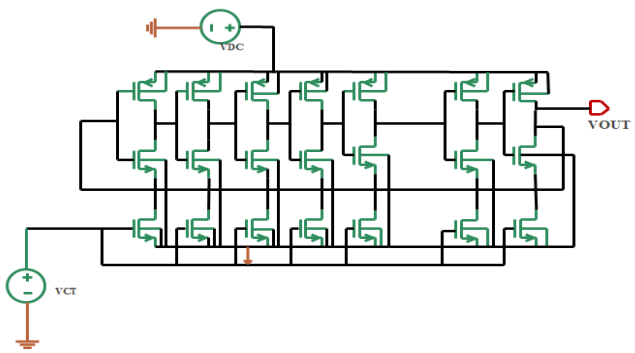

Fig.4.Schematic of proposed CMOS ring oscillator

Figure [4] describes the operation of proposed CMOS ring oscillator. There are seven-stage CMOS inverters shown in the diagram up there. It has a length of 45 nanometers, a width of 210 nanometers, and a thickness of 145 nanometers for PMOS and NMOS, respectively. The propsed method contains 21 transisitors in that T1 and T2 forms a invertor circuit which pbehaves the similar oprtaions of CMOS inverter and same T3 and T4 and vice versa.

V. IMPLIMENTATION OF CMOS RING OSCILLATOR

Each stage operation

The proposed votgae control oscillator contains odd number of 7 stages, 7 inverters connected in ring format. In first stage (T_1 and T_2) the input of the DC signal complemented with out distortion and converted to AC signal with condtions of oscialloins, and applied to the second stage, the signal strength is increased by composing of Common source amplifier (T_{15}) design providing 180˚ Phase shift. Due to odd number of stages the net phase shift produced is around 180˚, its mandatary to prouduce oscialltions. In second stage (T_3 and T_4) the input of the signal complemented and applied to the third stage (T_5 and T_6) with some dealy, the signal strength is increased by composing of Common source (T_{16}) amplifier design. Due to odd number of stages the net phase shift produced is around 180˚. At fourth stage (T_7 and T_8) of the input of the signal complemented and applied to the fifth stage with some dealy, the signal strength is increased by composing of Common source (T_{17})

amplifier design. Due to odd number of stages, the net phase shift produced is around 180˚, its mandatary to prouduce oscillations. At fifth the input of the signal (T9 and T10) complemented and applied to the sixth stage with some delay; the signal strength is increased by composing of Common source (T18) amplifier design. Due to odd number of stages, the net phase shift produced is around 180˚, its mandatary to produce oscillations. In sixth the input of the signal (T11and T12 with) CS amplifier (T20) complemented and applied to the seventh stage (T13 and T14) with some delay; the signal strength is increased by composing of Common source (T21) amplifier design. Due to every stage has inverter combinations with adjacent schematic with that it will produce oscillations. In order to drive the transistors, the NMOS and PMOS dimensions are crucial. In order to manage the inverter-based scheme mentioned before, a control voltage of 5V D.C. is required. As a result, the performance results and requirements should guide the parameter selection process. In the common source architecture of complementary metal-oxide semiconductors (CMOS), capacitance increases as frequency rises. A decrease in the supply voltage (VDD) causes the CMOS's phase noise to rise. Therefore, the CMOS device's sensitivity to supply changes should be the principal design parameter. Potential formulations include these. The frequency that results from running the suggested design is shown in the schematic below.

VI.SIMUALTION RESULTS

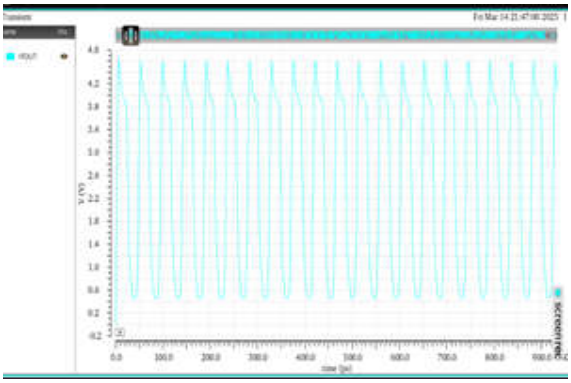

Fig.5.Simulation results of Proposed CMOS ring oscillator

The above figure generated by virtuoso cadence environment using CMOS Technology. Figure [5] describes the Simulation results of proposed CMOS ring oscillator. The suggested CMOS ring oscillator's simulation results are shown in the figure above. The frequency that the projected ring oscillator achieved was 21.6626 gigahertz. We can reduce noise by using longer channel lengths (L) and larger W/L ratios [8]. Determining the operating frequency alone by observing the CMOS's capacitance variations is not feasible due to other factors. It is important to choose the individual capacitors correctly so that any extra capacitance created by the frequency selections may be accounted for. When deciding on a frequency, there are a lot of factors to consider. As mentioned before, these parameters rely on the saturation of the used CMOSs and the functioning of an oscillator. The following graphic shows the frequency production of the proposed CMOS ring

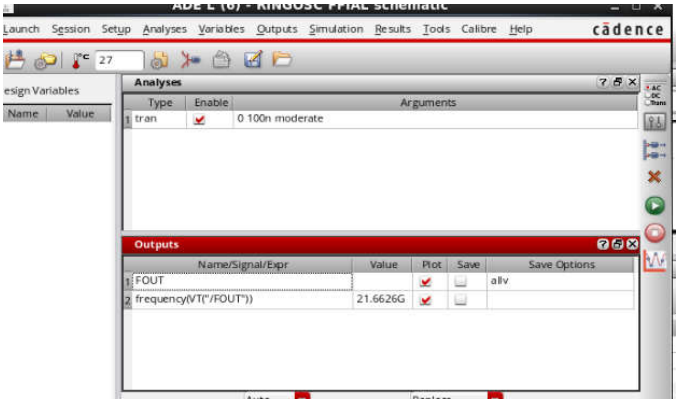

Fig.6. frequency measurement of proposed CMOS ring oscillator

Figure [6] describes the frequency measurement of proposed CMOS ring oscillator. The suggested ring [9] oscillator's simulation results are shown in the above figure. The frequency that the projected ring oscillator achieved was 21.6626 gigahertz. The frequency selection may be expressed in the following way: An increase in voltage causes an increase in the operating frequency. By modifying the capacitance delay, as shown in Equation 5, the frequency may be varied by varying the capacitors. On the other hand, the saturation level of the CMOSs in use limits this. The usage of the oscillator is the primary limitation on the practical choice of frequency. Because some applications need certain frequencies, careful frequency selection is essential. The application is the primary limitation of frequency selection, as previously mentioned. All of the other variables that affect frequency may be eliminated by using the right capacitors and power supplies. Figure below shows the results of the static and dynamic poweranalysis.

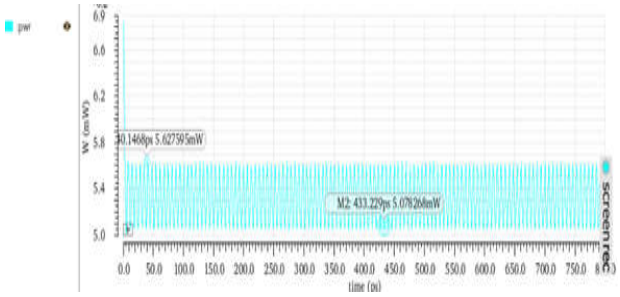

Fig.7. Power analysis of proposed CMOS ring oscillator

Figure [7] describes about the Power analysis of proposed CMOS ring oscillator. Analyzed in the figure above is static and dynamic power. This method's static power usage is 5.62 milliwatts. The suggested approach has a dynamic power usage of 5,078 milliwatts [10]. The number of stages is a very unstable design parameter for CMOS ring oscillators. Modifying the number of stages has a substantial impact on power, frequency, and noise, whether it's raised or lowered. Next, we have the power analysis happend

Comparison between existed and proposed results

Table1:

The below table [1] describes the various existing ring oscillators with proposed CMOS voltage [11] ring oscialltors designed with 7 stage CMOS ring socialltor architecture

S.No	Methods	Static Power	Dynamic Power	Average Power	Frequency GHz
1	Current Starved (uw)	561.33	561.93	561.9	2.3
2	Negative Skewed (mW)	5.257	5.257	5.258	3.35
3	Proposed Method (mW)	5.39	4.927	4.9	20

Figure [8] describes the Current straved [13] mechansoam have been utilized for generationg volateg ring oscllatior results in more power consumption. The Negative stratved [14-15] architecture has been deployed to generate oscillations results in more average power consupmtions.

II. CONCLUSION And Future Scope

For 5G standard mobile communication, this transceiver employs a very fast settling time VCO and a very broad tuning range. This VCO should preferably also have low-phase noise for best performance. The chain of inverters with transistor length optimization has improved the performance of the suggested scheme. Variations in the voltage technique have produced reliability. Seven hard number stages have embraced the suggested approach to improve accuracy.This need has prompted the development of tiny, battery-powered circuits that are perfect for Internet of Things (IoT) applications and 5G technologies; ring oscillators based on Very Large-Scale Integration (VLSI) are one such solution. Smart homes, smart cities, smart cars, smart grids, and health care services are all within reach. The recommended method uses 5.0 mW on average, 5.62 mW dynamic, and 5.0 mW static power. In the K Band spectrum, the proposed method may provide a frequency of 21.66 GHz. By combining several different architectural styles, the current starving design was able to produce the lowest feasible harmonic distortion; however, this came at the expense of a smaller frequency range and more space needs.

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