VERIFICATION AND SIMULATION OF LOW POWER AND HIGH EFFICIENCY 4X16 DECODER USING CMOS TECHNOLOGY

Kuram Deepthi[1] Dr. Srinivas Bachu[2]

Siddhartha Institute of Technology & Sciences, Narapally village, Peerzadiguda, Hyderabad, Telangana 500088

ABSTRACT

The inscription explores the layout of digital decoders, particularly the 4 × 16 and 3 × 8 decoders' attachments. This design approach analyzes several sensing gates and 2 × 4 decoders. Additionally, it delves into the use of CMOS technology, which is widely known for its quick speed and economical power operation, to a 4 × 16 decoder employing a 3 × 8 decoder. Using 26 transistors and mongrel approach, the suggested system uses a 2x4 decoder to create a 3x8 decoder. The suggested setup makes use of CMOS technology, a binary value sense, and a transmission gate. This setup significantly reduces the circuit complexity of the proposed device. The writers demonstrate mastery of the meter Virtuoso 45 GPDK software by effectively using it for circuit consumption and assessment. We have strictly enforced the use of 26 transistors in the suggested decoder. Every decoder design is based on CMOS technology has its power consumption properties measured properly. Based on the data, we conduct a comprehensive relative analysis that delves into the intricate relationship between power efficiency and circuit armature. The study offers insightful information for choosing decoders carefully, helping circuit designers create infrastructures that efficiently use energy while remaining operational. It advances the understanding of energy-efficient digital circuitry among academics. by providing a thorough insight into power consumption patterns. With any luck, this research will pave the way for future innovations and improvements in CMOS-grounded decoding circuits.

KEYWORDS: Decoder 2x4, 3X8 Decoder , low power ,High Speed.

I.INTRODUCTION

Improving performance while decreasing power consumption is the top priority while working with digital circuits. Digital decoders, which care about efficiency in operations and design, are what we're aiming for. This article discusses the intricate building of The 4 × 16 and 3 × 8 decoders are two significant decoder designs. [1]. In the design phase, the inquiry examines the use of different logic gates and how to integrate 2 × 4 decoders. Constructing a 4 × 16 decoder from a 3 × 8 decoder is the primary objective of the study. Utilizing the most advantageous aspects of CMOS technology, this approach makes use of its rapid

processing speed and low power consumption. Power consumption, and more The main emphasis of the study is on the different [4-5]architectural configurations of digital decoders. The study's conclusions emphasize the importance of CMOS-based decoders and their energy efficiency. The authors' careful use of Cadence Virtuoso software demonstrates their expertise in circuit design and testing [2]. Creating and modeling decoder circuits with a systematic way is the main focus of this work. With circuits standing in for many architectural paradigms, designers have a world of possibilities at their fingertips. The study examines the power consumption features of every decoder architecture in detail [10]. The use of complementary metal-oxide semiconductors (CMOS) strengthens the project and enables a more thorough comparison. This research provides valuable insights beyond just numerical data by examining the impact of circuit arrangement on power efficiency. Going beyond quantitative analysis to include qualitative factors, the book examines the relationship between logic gate designs and transistor networks [3]. This research examines the significant impact these components have on power consumption. Beyond the theoretical, this research provides actionable recommendations for decision-makers [8–10]. Prioritizing energy economy while ensuring the circuit operates is the top priority for circuit designers. After examining theoretical foundations, this article goes on to discuss potential applications. This movie does a fantastic job of connecting theoretical discussion with practical applications via its multiple decoder designs. Section I is where this investigation begins. Section II: Reviewing the Existing Literature. Section Three. Standard Procedure 1. Section 4 lays out the recommended method, and Section 5 concludes by outlining the next steps.

II.LITERATURE SURVEY

In integrated circuits, most logic gates are static CMOS circuits. Built from nMOS pull down and pMOS pull up networks, which function together, they provide great performance and are resistant to fluctuations caused by noise and devices. Consequently, CMOS logic can withstand voltage scaling and shrinking transistor sizes, enabling it to reliably operate at low voltages. Very large scale integration (VLSI) relies on static CMOS circuitry. With nMOS serving as the pull-down and pMOS as the pull-up networks, CMOS circuits are able to improve efficiency and noise resistance. Reduced transistor size, simple transistor sizing, voltage scaling, and excellent performance at low voltages are other advantages of complementary metal-oxide semiconductor logic. According to Moore, the deity of Intel, the density of transistors on integrated circuits (ICs) has increased every year since their conception. Unfortunately, Moore's law has become irrelevant due to the slowed pace and the fact that data density doubles every 18 months. Improvements in very large scale integration (VLSI) technology have made it possible to fabricate billions of transistors on a single chip.

Power consumption Therefore, there is a need for VLSI technology. For very large scale integration (VLSI) technologies, there are several design stages. These levels include architectural, process technology, layout, and circuit. The circuit level design offers considerable power savings by selecting an appropriate logic style for implementing combinational circuits. A major issue in the realm of innovation is the current decrease of energy. Low power configuration is a major issue in high-end, complex frameworks like semiconductors [6] and digital signal processors (DSPs). Emergence of very complex circuits with high clock frequencies is a direct result of improvements in working speeds and chip thickness. Mechanical design of low power VLSI circuits is required by the proliferation of practical consumer goods. A decoder is a combinational logic circuit that takes a pair of numbers and an incentive and turns them into an example of a relevant yield bit. Decoders have several uses, such as interpreting memory addresses, de-multiplexing information, displaying seven parts of a matrix, and many more.

III.EXISTING METHOD

This study examines digital decoder design in depth, including several configurations and their effects on circuitry and functioning. This academic study examines many decoder types, including the 4 × 16 decoder that utilizes 2 × 4, the 3 × 8 decoder that employs 2 × 4 pieces, a unique 2 × 4 decoder that employs distinct logic gates, and an innovative take on the 4 × 16 decoder that incorporates a 3 × 8 decoder. Figures 1, 2, 3, and 4 display these designs in that order. Power consumption analysis is a key component of developing energy-efficient circuit designs, and this study examines it. To determine the power consumption of each circuit, we used power calculation algorithms. The calculations give a solid foundation for comparing the power effectiveness of various decoder designs. The study explores the complex connections between transistor networks, power consumption, [7] and, logic gate topologies, and more. The results of this investigation, which relies on CMOS technology, are very helpful. Start up of the 2X4 decoder. A digital circuit known as a 2x4 decoder with an enable pin may receive a 2-bit binary input and, depending on the input combinations, produce one of four outputs. Toggle the circuit's on/off status using the enable pin.

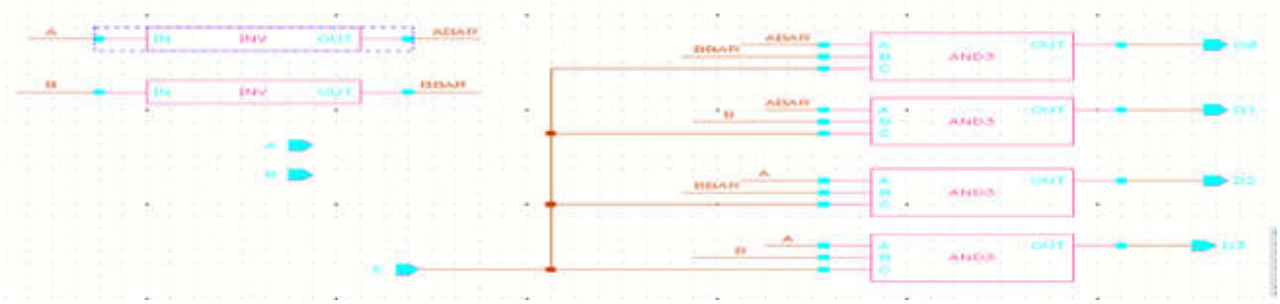

Fig1.Schematic of 2X4 decoder with enable pin

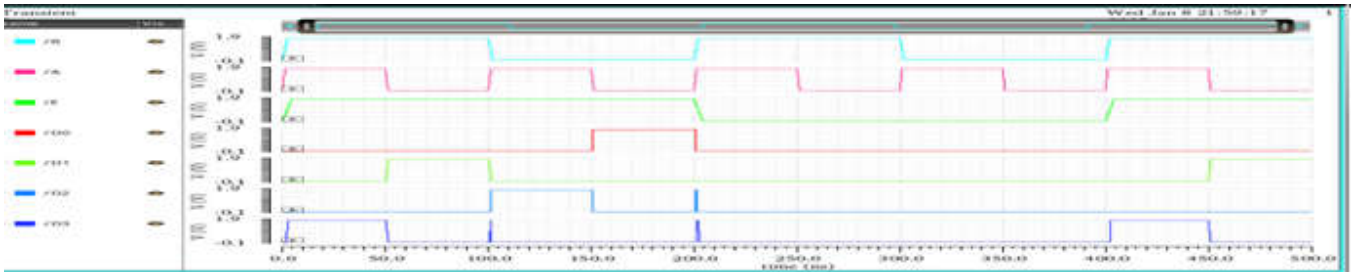

Fig.2.Simulation of 2X4 decoder with enable pin.

A CMOS 3x8 decoder using two 2x4 decoders with enable pins works by cascading smaller decoders and controlling their activation based on the most significant input bit. The principle involves splitting the input logic and selectively enabling one of the two 2x4 decoders [8] at a time, thus generating the required 3-to-8 decoding functionality

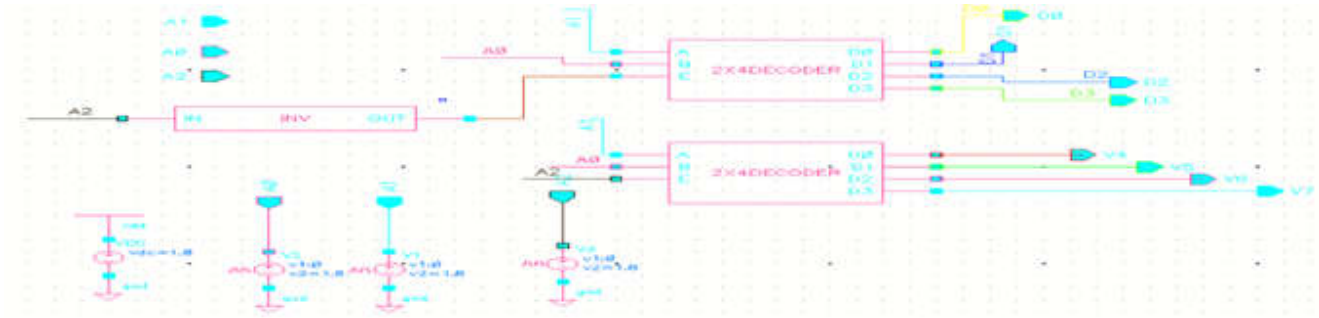

Fig.3.Schematic of 3X8 decoder with enable pin

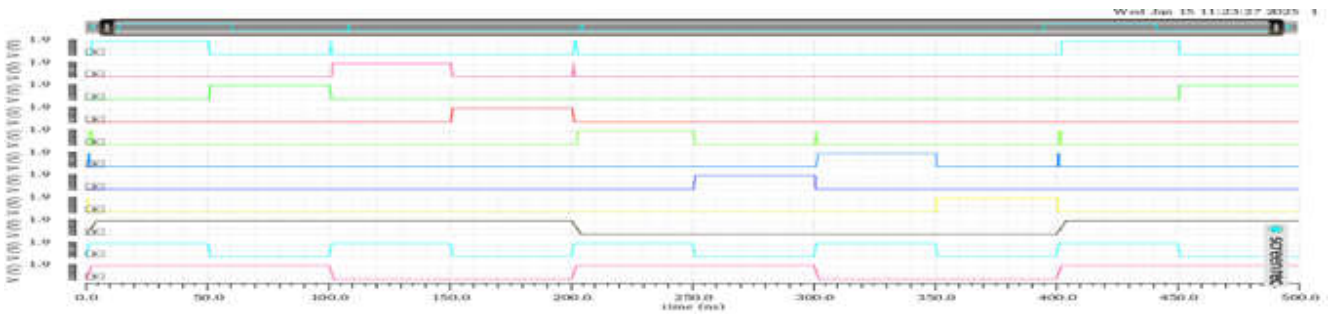

Fig.4. Simulation of 3X8 decoder with enable pin

4X16 DECODER DESIGN USING 2X4 DECIDER

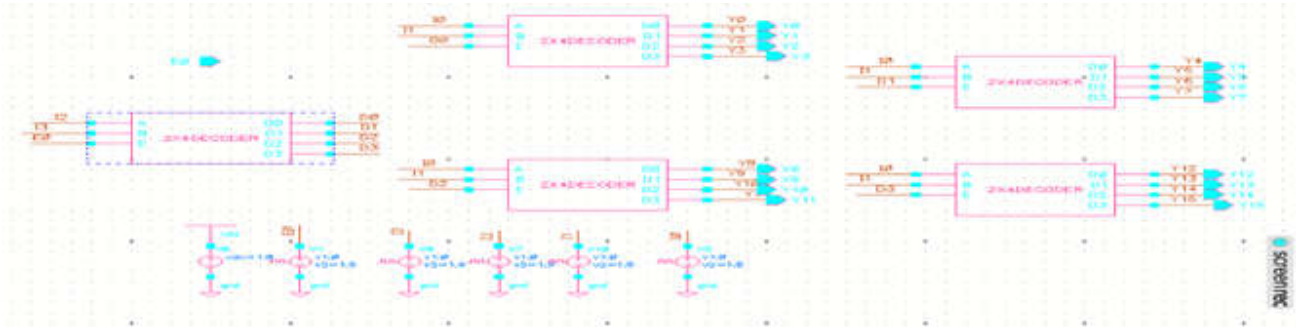

Fig.5.A 4-to-16 decoder can be designed using five 2-to-4 **decoders** with enable signals.

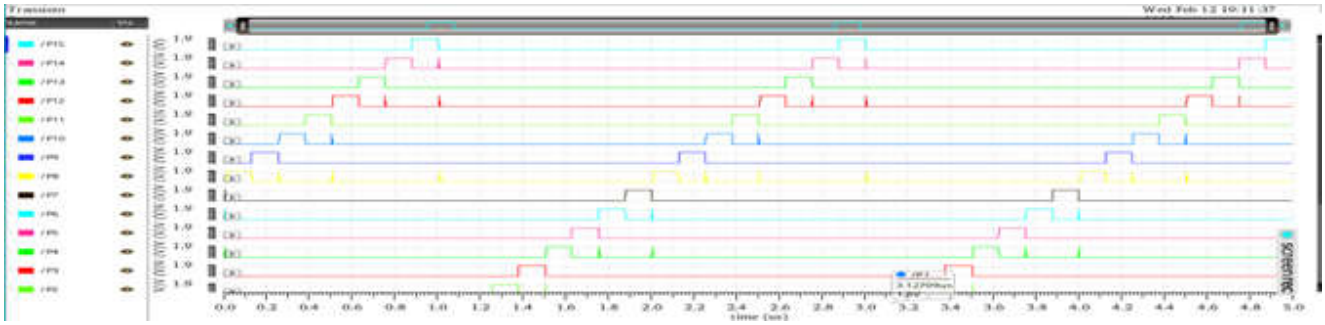

Fig.6.Simulation of A 4-to-16 decoder can be designed using five 2-to-4 decoders with enable signals

IV.PROPOSED METHOD

Proposed method 26 Transistor Decoder using 2x4 [9] decoderIt would take a total of 26 transistors to design a 2–4 line decoder using either TGL or DVL gates (18 for AND/OR gates and 4 for inverters). It is feasible to remove one of the two inverters, bringing the total number of transistors down to 26 by combining both AND gate types into the same topology and using the appropriate signal arrangement.

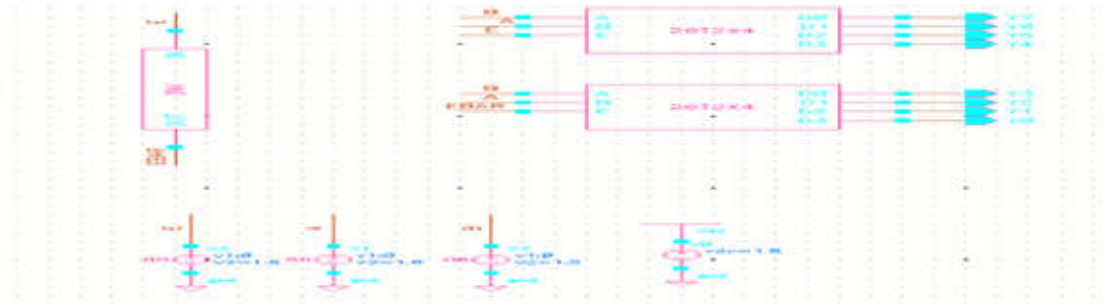

Fig.7.Proposed method 26 Transistor Decoder using 2x4 decoder

Assume that we want to remove the B inverter from the circuit out of the two inputs, A and B. Using A as the propagate signal, a DVL gate is utilized to implement the Do min-term (AB). B serves as the propagate signal in the implementation of the D1 min-term (AB) using a TGL gate. Using A as the propagate signal, a DVL gate is utilized to implement the D2 min-term (AB). Lastly, a TGL gate is employed to construct the D3 min-term (AB), [10] with B serving as the propagate signal. These specific decisions totally avoid using the complimentary B signal.

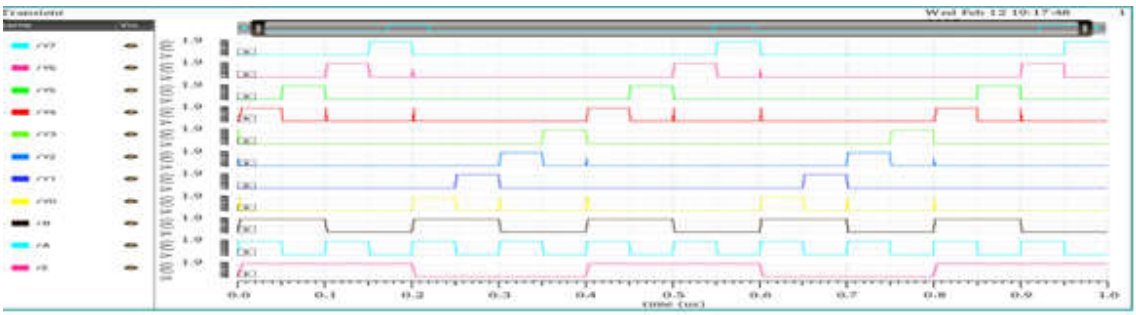

Fig.8.Simulation of Proposed method 26 Transistor Decoder using 2x4 decoder

DPL and DVL are examples of devices that employ both nMOS and pMOS pass transistors. DVL is the type we look at in this study. It keeps the full swing action of DPL but uses fewer transistors. Figure shows the 2-input DVL AND/OR gates, one for each kind. They are full swinging, but they don't restore. The TGL/DVL[12] gates only need three transistors if they have the right inputs. Decoders have high fan-out circuits, which means that numerous gates may utilize the same few inverters. This means that employing TGL and DVL can lower the number of transistors needed. One thing that all of these gates have in common is that they are not balanced, which means that their input loads are not the same on both sides. We designated the two gate inputs X and Y, as shown in Figure 3. Input X controls the gate terminals of all three transistors in TGL gates. Input Y, on the other hand, passes via the transmission gate to the output node. In DVL gates, input X controls two transistor gate terminals, while input Y controls one gate terminal and sends the signal to the output via a pass transistor. We shall call X and Y the gate's control signal and propagation signal, respectively.

COMPARISON TABLE ANALYSIS:1

S.no	Implementation of decoder	Power consumption (in µwatts)
1.	2 × 4 Decoder	1.298
2.	4 × 16 at 3 × 8	4.8
3.	3 × 8 at 2 × 4	6.10
4.	4 × 16 at 2 × 4	9.56
5.	3 × 8 at 2 × 4 (This work)	466.6 × 10–12

. In proposed method the minimum power consumption 1.836 Nano watt and maximum power consumption becomes 307.202 micro watt. The proposed design shows that the average power consumption is going to very less compared to existing methods. The proposed method of 3x8 decoder using 2x4 decoder designed with 26 transistors with hybrid methodology. The proposed method has been design with transmission gate, dual value logic [13] and CMOS method. With this configuration the proposed method circuit complexity becomes very less.

V.CONCLUSION AND FUTURE SCOPE

Here, we examined the decoder design and all of its intricate components. Through meticulous research and preparation, we have identified key characteristics that will propel this vital field ahead. We analyze decoder configurations in detail to determine their efficiency and power consumption. Our The most important component of the results is the power analysis for each decoder architecture. Because of its hierarchical structure and several cooperative decoding layers, the 4 × 16 decoder is notorious for using a lot of power. Because it employs a composite decoding technique, the 3 × 8 decoder with 2 × 4 decoders is better than finds a middle ground between being complicated and conserving energy. The 2 × 4 decoder exemplifies efficient energy use, highlighting the inherent beauty in basic circuit design. An excellent combination of complexity and energy efficiency is the 4 × 16 decoder, which consists of 3 × 8 decoders. Research like this bridges the gap between theory and practice, putting conceptual knowledge to good use. Findings from this study may inspire novel approaches to building decoders with reduced power consumption. There will likely be far-reaching consequences for digital circuitry, particularly CMOS-based decoding circuits. Future work on "Designing of Power-Efficient CMOS Based Digital Decoder: Architectural Variations and Comparative Insights" may cover a lot of ground, including exciting new developments in the field. Beyond Fin-FET: The following is an agenda item: Considering the power requirements and growth potential of Fin-FET, GAAFET, and other contemporary CMOS technologies, examine their potential applications in digital decoders. Operation Looking into decoders that operate below the threshold voltage entails investigating circuits that operate at voltages lower than the threshold value. This significantly reduces electricity consumption. Novel compounds.

REFERENCES

[1] F. Al-Jame, R. A. Al-Fares, W. Ali, H. Ashour, and N. Murshid, "Journal of VLSI Circuits and Systems," Journal of VLSI Circuits and Systems, vol. 5, no. 1, pp. 55-60, 2023.

[2] Xue, X., Sai Kumar, A., Khalaf, O. I., Somineni, R. P., Abdulsahib, G. M., Sujith, A., Dhanuja, T., & Vinay, M. V. S., "Design and Performance Analysis of 32 × 32 Memory Array SRAM for LowPower Applications," Electronics (Switzerland), vol. 12, no. 4, 2023.

[3] Prasad, V., Banerjee, A., & Das, D., "Design of ternary encoder and decoder using CNTFET," International Journal of Electronics, vol. 109, no. 1, pp. 135-151, 2022.

[4] Ramakrishna Gadde, G., "Optimization of Area, Power, and Delay in BCD to Seven segment decoder using MGDI Technique," International Journal of Advances in Engineering and Management (IJAEM), vol. 3, 2021.

[5] Preethi, D., Valarmathi, R. S., & Harikumar, R., "Energy efficient VLSI decoder chip with reduced PAPR in FECG monitoring," International Journal of Electronics, vol. 107, no. 8, pp. 1304-1323, 2020.

[6] Paganoti De Almeida, D., Schuertz, J. R., Batista, S., & França, L., "A Building Block VLSI Design of an Information Decoder Using VHDL," n.d, 2019.

[7] Rajeev Ratna Vallabhuni, J. Sravana, M. Saikumar, M. Sai Sriharsha, D. Roja Ran, "An Advanced Computing Architecture for Binary to Thermometer Decoder using 18nm FinFET," Proceedings of the 3rd International Conference on Smart Systems and Inventive Technology (ICSSIT 2020), 20-22, August 2020.

[8] Rohit Kumar Arya, Sonali Agrawal, "Design of Efficient 2-4 Modified Mixed Logic Design Decoder," Proceedings of the 4th International Conference on Communication and Electronics Systems (ICCES 2019), 17-19, July 2019.

[9] N. S. Sumana, B. Sahana and A. A. Deshapande, "Design and Implementation of Low Power - High Performance Mixed Logic Line Decoders," 2019 4th International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT), Bangalore, India, 2019, pp. 529-534.

[10] P. K. Patel, M. Malik, T. K. Gupta, "Optimization Techniques for Reliable Low Leakage GNRFET-Based 9T SRAM," IEEE Transactions on Device and Materials Reliability, vol. 22, no. 4, pp. 506-516, Dec. 2022.

[11] J. S. Gomes, R. N. Wuerdig, F. L. L. Ramos, S. Bampi, "AV1 Residual Syntax Elements Assessment and Efficient VLSI Architecture," 2023 36th SBC/SBMicro/IEEE/ACM Symposium on

Integrated Circuits and Systems Design (SBCCI), Rio de Janeiro, Brazil, pp. 1-6. 2023.

[12] M. N. G. Prasad, K. E. Sreenivasa Murthy, K. Prasad Babu, "A Study & Analysis on low Power processor Design Using Various Techniques," Tuijin Jishu/Journal of Propulsion Technology, Sep. 11, 2023.

[13] N. S. Dhakad, E. Chittora, G. Raut, V. Sharma, S. K. Vishvakarma, "In-Memory Computing with 6T SRAM for Multi-operator Logic Design," Circuits, Systems, and Signal Processing, Aug. 19, 2023.